

## Refine Search

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### Search Results -

Term	Documents
EVENT	406356
EVENTS	106103
MICROPROCESSOR	154967
MICROPROCESSORS	34270
TRACE	111985
TRACES	70218
HANDLER	15914
HANDLERS	5273
((TRACE ADJ HANDLER) AND (EVENT ADJ MICROPROCESSOR)).USPT.	0
(EVENT ADJ MICROPROCESSOR AND TRACE ADJ HANDLER ).USPT.	0

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<b>Database:</b>	<input checked="" type="checkbox"/> US Pre-Grant Publication Full-Text Database <input type="checkbox"/> US Patents Full-Text Database <input type="checkbox"/> US OCR Full-Text Database <input type="checkbox"/> EPO Abstracts Database <input type="checkbox"/> JPO Abstracts Database <input type="checkbox"/> Derwent World Patents Index <input type="checkbox"/> IBM Technical Disclosure Bulletins
<b>Search:</b>	<input type="text" value="L26"/> <span style="float: right; margin-top: -20px;"> <b>Refine Search</b> </span>
<input style="margin-right: 20px;" type="button" value="Recall Text"/> <input style="margin-right: 20px;" type="button" value="Clear"/> <input style="margin-right: 20px;" type="button" value="Interrupt"/>	

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### Search History

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**DATE:** Friday, April 16, 2004    [Printable Copy](#)    [Create Case](#)

**Set Name** **Query**  
side by side

**Hit Count** **Set Name**  
result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L26</u>	event adj microprocessor and trace adj handler	0	<u>L26</u>
<u>L25</u>	event adj CPU and trace adj handler	0	<u>L25</u>
<u>L24</u>	L23 and trace adj handler	0	<u>L24</u>

<u>L23</u>	event adj processor	1108	<u>L23</u>
<u>L22</u>	L2 and trace adj handler	1	<u>L22</u>
<u>L21</u>	L20 and trace adj handler	0	<u>L21</u>
<u>L20</u>	event adj processor	1108	<u>L20</u>
<u>L19</u>	event adj processor and trace adj handler	0	<u>L19</u>
<u>L18</u>	L12 and layer	2	<u>L18</u>
<u>L17</u>	L6 and layer	0	<u>L17</u>
<u>L16</u>	L12 and protocol adj layer	1	<u>L16</u>
<u>L15</u>	L12 and optimization	1	<u>L15</u>
<u>L14</u>	L12 and stack	1	<u>L14</u>
<u>L13</u>	L12 and protocol adj stack	1	<u>L13</u>
<u>L12</u>	trace adj handler and event and trace	6	<u>L12</u>
<u>L11</u>	event adj trace and even adj processor	0	<u>L11</u>
<u>L10</u>	L9 and protocol adj optimization	1	<u>L10</u>
<u>L9</u>	create adj intermediate and protocol and optimization	18	<u>L9</u>
<u>L8</u>	L7 and intermediate	1	<u>L8</u>
<u>L7</u>	L4 and create	11	<u>L7</u>
<u>L6</u>	L4 and creation	0	<u>L6</u>
<u>L5</u>	L4 and layered adj protocol	1	<u>L5</u>
<u>L4</u>	L3 and overhead	16	<u>L4</u>
<u>L3</u>	L2 and performance	63	<u>L3</u>
<u>L2</u>	optimized adj protocol	117	<u>L2</u>
<u>L1</u>	Ranesse and event adj traces	0	<u>L1</u>

END OF SEARCH HISTORY